Low phase noise LC-VCO with and multi-stage filtering

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Abstract: A low-phase-noise CMOS voltage-controlled oscillator (VCO) with zero-bias scheme and multi-stage filtering is presented. Sharing ground with fully integrated loop filter, the PMOS-only VCO achieves a zero-bias scheme, which prevents tuning line noise from disturbing VCO output common-mode voltage and hence minimizes phase noise caused by nonlinear C-V characteristic of varactors. Top-biased current source is optimized by multi-stage filtering to reduce 1/f flicker and thermal noise. Fabricated in TSMC 180 nm CMOS process, the proposed VCO exhibits a measured oscillation frequency of 0.85~1.45 GHz, with a phase noise of -121.8~-131.3 dBc/Hz @1MHz offset over the whole band. Power consumption is 3.8~6.3mW from a 1.8V supply.
Keywords: LC Oscillator; PMOS-only; VCO; Low Phase Noise; Wideband

1 Introduction

Wireless networks for Industrial Automation (WIA) based on IEEE 802.15.4-2006, is proposed by China for wireless industrial applications[1, 2]. Voltage-controlled oscillator (VCO) used for WIA transceiver features wideband, low phase noise, and low power. Recently, many works[3, 4, 5, 6] focus on wideband and low phase noise VCO design. Ref.[3] utilizes a switchable active core to achieve wide band at little expense of power consumption and phase noise aggravation. A tailor-made sub-nH high-Q inductor is employed in[4] to realize wideband and low phase noise. Ref.[5] uses a 7-bit binary-weighted capacitor array to attain low tuning sensitivity. Active-inductor based noise filters are presented in[6] to reduce phase noise. The above-mentioned works suffer from unavailable customized device and noticeable circuit complexity. This paper proposes simple and practical methods which are zero-bias scheme and multistage filtering. With these techniques, the proposed VCO achieves an oscillation frequency of 0.85~1.45 GHz and a phase noise of -121.8~-131.3 dBc/Hz @1 MHz offset over the entire band. This VCO has successfully applied to the WIA transceiver.

2 Circuit design

Fig. 1 depicts the proposed PMOS-only LC-VCO which consists of a top-biased current source, a cross-coupled PMOS pair, a switched capacitor array (SCA), a self-controlled varactor array (SVA), a continuous tuning cell and a symmetrical inductor. PMOS-only type is adopted due to the low 1/f noise, good substrate isolation, and excellent supply noise suppression[7]. For reliable start-up over wide band and low phase noise[8], current source is adjustable by a current array controlled by digital code. A 4-bit binary-weighted SCA[3] with 16 tuning curves is utilized to cover a wide band. A 2-bit binary-weighted self-controlled SVA[9] is used to suppress the tuning sensitivity fluctuation. To maximize linear range of each tuning curve, distributed-bias technique[10] is adopted for varactors. The simulated voltage of "vb0" and "vb1" are 0.52 V and 1.28 V, respectively, leading to a wide linear range of 1.4 V. "vb3" is 1.6 V to reversely bias the varactor if the SVA cell is switched out of the tank. The spiral inductor has an octagonal shape and is implemented in the thick top (2.34um) metal layer.

Instead of usingdifferential tuning technique to minimize the impact of tuning line noise[11], this paper proposes a zero-bias scheme, which suits the circumstances when the output of loop filter is single-ended. It is realized by grounding the center tap of the symmetrical inductor and sharing the ground with

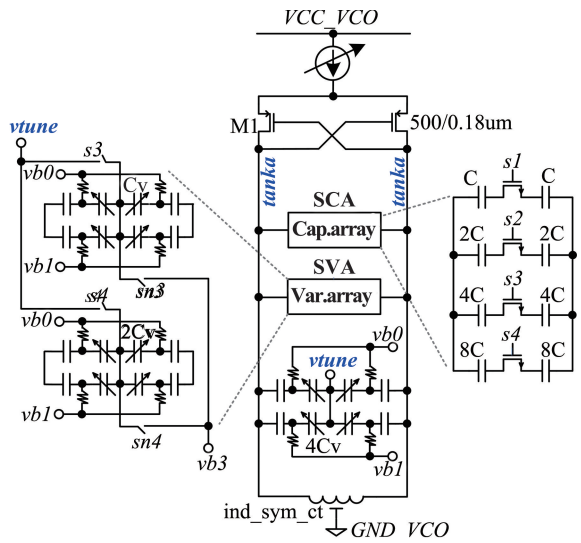

Fig. 1 Proposed low phase noise PMOS-only LC-VCO.

the fully-integrated loop filter, as shown in Fig. 2 (a). The common ground is directly connected to wire-bonding pad for minimizing coupling noise from surrounding circuit and substrate. At DC and low frequency, VCO output bias is about zero, which effectively prevents the tuning line noise from polluting the VCO output common-mode (CM) voltage. Since any variation of CM voltage can translate to phase noise through the nonlinear C-V characteristic of varactors[7], this scheme can reduce the VCO phase noise.

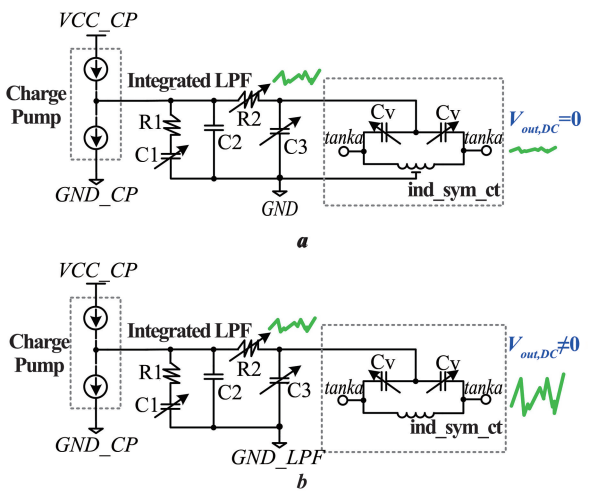

Fig. 2 Tuning line noise impacts on VCO output common-mode voltage. (a) Zero-bias scheme (b) Non-zero-bias scheme

For vivid contrast, Fig.2 (b) illustrates a non-zero-bias scheme. The DC bias of VCO output is not zero. In this scheme, a capacitance divider emerges if travelling from the VCO output terminal to the loop filter's ground. The divider is mainly formed by the varactor "C_v" and the capacitor "C_3". As manifested by Eq. (1), the tuning line noise "V_n" is considerably amplified when it appears at the VCO output terminal, which aggravates VCO phase noise.

$$V_{out,p,n} = V_n \frac{C_v + C_3}{C_v} \quad (1)$$

Multi-stage filtering is presented in current source to reduce 1/f and thermal noise, although some preliminary measures have been taken to minimize the noise, as shown in Fig. 3. The measures are: 1) using an internal bandgap to purify the reference current; 2) channel length of M0~M4 and M8~M10 are 10 μm and 4 μm, respectively; and 3) M11 uses a moderate length (0.5μm) to achieve a balance between parasitic capacitance and flicker noise. As for multi-stage filtering, MOS capacitor C0 filters out the M3 noise; C1 sifts the M8 noise; R1 and C2 constitute an ultralow pass filter to lower the M10 noise. Considering the silicon area, all of the capacitors are implemented by MOS transistor.

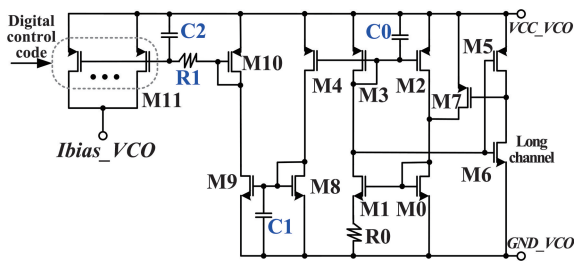

Fig. 3 Multi-stage filtering applied to the top-biased current source.

In Fig. 3, C0 = C1 = 6.5 pF, C2 = 50 pF, R1 = 700 KΩ. Thus, f_{3dB} = 1 /(2π R1 * C2) = 4.55KHz, which is sufficiently low to attenuate M10 noise. The 1/f and thermal noise of current source is reduced, and hence the VCO phase noise is lowered[12], which is illustrated in Fig. 4. It shows post-layout simulation result from 1Hz to 100MHz offset using Cadence Spectre-RF simulator. When VCO os-

cillation frequency is 1.33GHz, the simulated phase noise is reduced by about 8.4dB, 9.9dB, 7.8dB at 10kHz, 100kHz, and 1MHz offset, respectively.

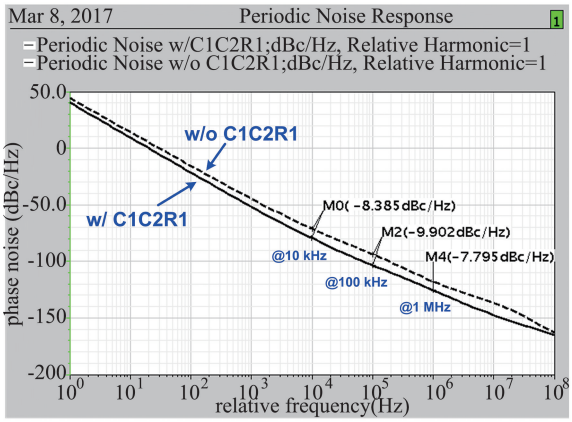

Fig. 4 Simulated phase noise reduction by multistage filtering technique at 1.33 GHz.

3 Experimental results

To evaluate theproposed VCO performance, the chip was fabricated in TSMC 180 nm CMOS technology. Fig. 5 shows the die photograph that occupies an active area of 0.6mm^2.

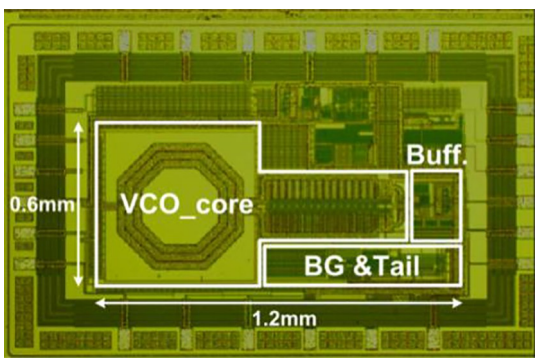

Fig. 5 Die micrograph of the proposed VCO.

The VCO chip was mounted on a printed circuit board (PCB) by wire bonding, as shown in Fig. 6. The VCO dissipated 3.8~6.3mW from a 1.8V supply including output buffer.

Fig. 7 depicts the test setup of the proposed VCO. Using apower supply and a Rohde & Schwarz FSV signal analyzer, the VCO output spectrum, frequency tuning curves and phase noise can be measured one by one.

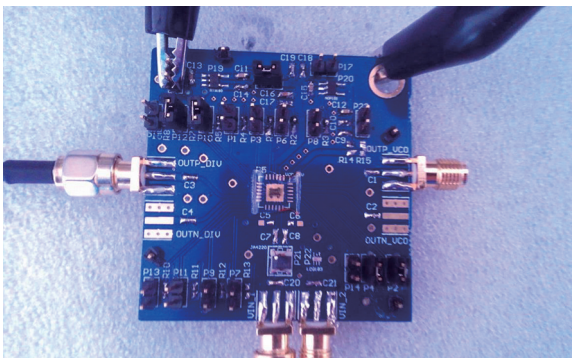

Fig. 6 PCB evaluated board of the proposed VCO.

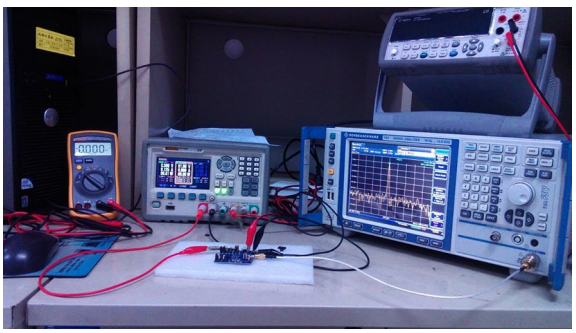

Fig. 7 Test setup of the proposed VCO.

The measured frequency tuning range was shown in Fig.8 by sweeping the switched capacitor array (SCA). The total frequency tuning range of the VCO was from 0.85GHz to 1.45GHz, resulting in a tuning range of 600MHz (52%). The tuning sensitivity of the proposed VCO changed from 35MHz/V to 70MHz/V.

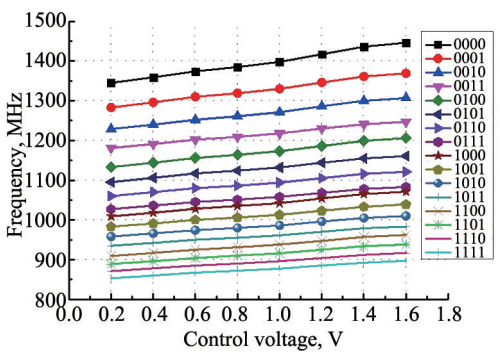

Fig. 8 Measured frequency tuning range of the proposed VCO.

Fig.9 shows that the measured single-sideband phase noise is at 1.05GHz, which is the typical oper-

ation frequency. As shown in Fig.9, the spot phase noise is -102.47 dBc/Hz and -125.19dBc/Hz at offsets of 100KHz and 1MHz, respectively.

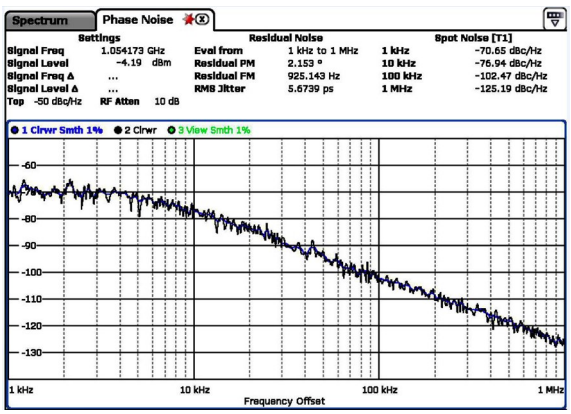

Fig. 9 Measured VCO phase noise at oscillation frequency of 1.054GHz.

Over the whole oscillation frequency band, the measured phase noise was -95.4~-105.1dBc/Hz and -121.8~-131.3dBc/Hz at 100kHz and 1MHz offset, respectively, which is shown in Fig.10. Both fluctuations are less than 10dB. The FOM (Figure-of-merit) value[7] through the full band is -179.1~ -181.7 @1 MHz offset.

$$FOM = L(\triangle f) - 20\log(\frac{f_0}{\triangle f}) \qquad (2)$$

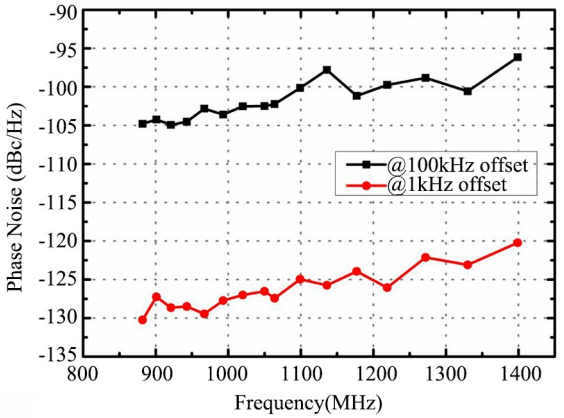

Fig. 10 Measured VCO phase noise throughout the whole band at 100KHz and 1MHz offset.

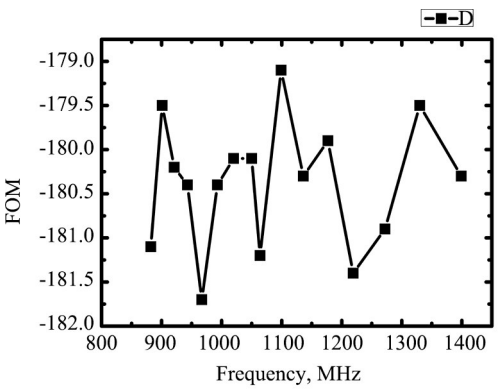

Fig. 11 Calculated FOM of the proposed VCO throughout the whole band at 1MHz offset.

Table 1 Performance comparison with prior wideband CMOS *LC*-VCOs

References	Technology (nm)	Tuning range (GHz)	Tuning range (%)	Phase Noise (dBc/Hz) @1 MHz offset	Power (mW)	Area (mm^2)	FOM_T
[3]	65	3.36~5.10	41	-123.1 @4.21G	8.7	0.24	-198.4
[4]	180	2.24~4.95	75	-130.8 @2.20G	32.4	0.51	-182.7
[5]	180	1.33~2.08	44	-123.4 @1.70G	18.0	0.34	-188.3
[6]	130	1.00~2.00	66	-120.0 @1.70G	2.1	0.11	-197.7
[8]	130	3.06~5.61	58	-120.8 @3.06G	3.0	0.3	-185.6
[9]	130	3.10~5.20	51	-119.0 @3.10G	9.2	NA	-179.3
This work	180	0.85~1.45	52	-131.3 @0.85G -121.8 @1.45G	3.8~ 6.3	0.6	-216.2 -211.3

Table 1 gives the performance comparison with other low phase noisewideband CMOS VCOs. The FOM_T (Figure-of-merit including tuning range) shown in Eq. (3) is widely used to evaluate the wideband VCO performance [12]. Comparison result shows that this work achieves low phase noise, wide tuning range, and low power consumption, leading to a better FOM_T.

$$FOM_T = L(\triangle f) - 20\log(\frac{f_0}{\triangle f}\frac{FTR}{10}) + 10\log(\frac{P_{DC}}{1mW}) \quad (3)$$

4 Conclusion

A low-phase-noise LC-VCO with zero-bias scheme and multi-stage filtering is presented. Zero-bias scheme suppresses the tuning line noise and hence minimizes the phase noise caused by nonlinear C-V characteristic of varactors. Multi-stage filtering in the optimized current source filters out the near-zero and $2\omega_0$ current noise and thus substantially reduces the VCO phase noise. Fabricated in TSMC 180 nm CMOS process, the proposed VCO exhibits a measured phase noise of -121.8~-131.3 dBc/Hz @1 MHz offset over the full band. The frequency range is 0.85~1.45 GHz.

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