Research of optical rainfall sensor based on CCD linear array

YANG Bifeng[1*], LIU Yuyan[1], LU Ying[2], WU Shangqian[3]

(1.*Chengdu University Of Information Technology*, *Chengdu* 610225; 2.*China Huayun Group*, *Beijing* 100081; 3.*Kunming University Of Science And Technology*, *Kunming* 650500)

Abstract: Rainfall monitoring is one of the most important meteorological observation elements for the disaster weather. The maintenance of current tipping bucket rain gauge and weighing type rain gauge is a critical issue. The optical rainfall sensor based on CCD linear array is mainly studied in this paper. Because of the maintenance-free time and good adaptability, it can be widely used in the automatic rainfall monitoring in severe environment and have a good perspective in using.

Key words: CCD linear array; raindrop spectrum; FPGA; dynamic threshold

1 Introduction

During the Twelfth Five-year Plan period, the government will increase investment on the monitoring and early warning of mountain flood and debris flow in the medium-sized and small-sized rivers. The maintenance of current tipping bucket rain gauge and weighing type rain gauge is a critical issue. Therefore, there are many restrictions for the application of these rain gauges in meagerly-populated, traffic inconvenient and poor natural environment conditions. Because of the maintenance-free time and good adaptability, the optical rainfall sensor can be widely used in the automatic rainfall monitoring in severe environment.

The basic principles of optical measurement and photoelectric detection are applied to precipitation observation, weather phenomenon observation and the physical structure of fog detection. The purpose is to study a new optical rainfall sensor with practical value and independent intellectual property rights, and provide a new technical means for the automatic measurement of rainfall and rain drops. It plays a key role in early warning of heavy rain, mountain flood and debris flow and other disasters, so this has a good perspective in using and application prospect. At the same time, the research results will help filling in a gap in this field and make a contribution to the localization of meteorological equipment.

2 System design

The current optical gauge/optical disdrometer can be divided into video camera and optical occlusion from detection methods. The former price is expensive and generally used for research. And the latter has relatively low price for observation [1]. The existing occlusion type optical rain gauge adopts one-dimensional test, whose sampling interval area is about $50cm^2$. Only the one-dimensional horizontal size of precipitation particles can be measured. A mathematical model is established for the conversion between horizontal scale of precipitation particles and size according to the hypothesis of particle vertical axisymmetric (The small particle is assumed to be a sphere, and the big particle is assumed to be a long ellipsoid or a flat circle.) to calculate the effective size and volume of precipitation particles and then estimate the precipitation. The main problem of this method is that the one-dimensional test and few detectors lead to little measurement information. One-dimensional test is contradictory between representation and particle mutual occlusion [2]. It is questionable that if the $50cm^2$ interval area is enough representative, which need further discussions. So the existing detection method is difficult to improve the detection accuracy. The basic idea of this design is to make full use of the advantages of the latest optical detection technology, and to improve the detection method based on the analysis of the advantages and disadvantages of the current technology. In order to accurately detect the volume of precipitation particles as the basic starting point, a two-dimensional test system is constructed to measure the two-dimensional scale and drop velocity of precipitation particles. It needs to increase the sampling area and the representation, and reduce the influence of the mutual occlusion of particles.

To achieve the above detection mode and measurement methods of two-dimensional scale and speed, the optical rainfall sensor system is intended to use, as shown in Fig 1. The combination of two-dimensional detection and high speed FPGA signal processing are the main feature of the system. The linear array detector has the fast enough time response characteristic, and it can completely meet the detection requirements of the 0.1mm particle size resolution. The two-dimensional detection is shown in Fig 2, the X and Y dimensional optical paths are used for precipitation particle size detection.

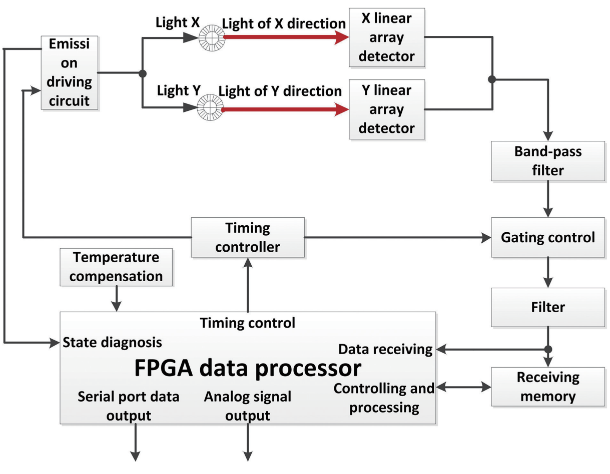

Fig. 1 Optical rainfall sensor system

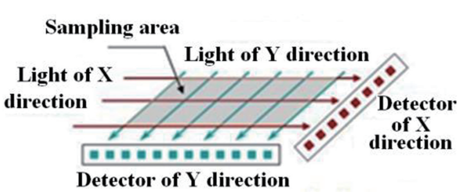

Fig. 2 Two-dimensional opticaldetection paths structure

3 Hardware design

The hardware of two- dimensional optical detection pathsare almost the same and this paper discusses one of these. And the hardware system diagram is shown in Fig 3.

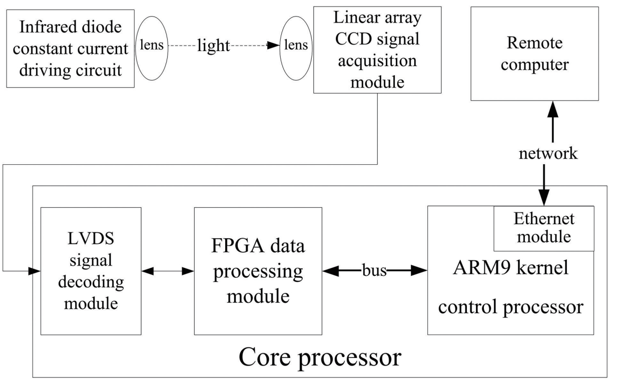

Fig. 3 Hardware system diagram

Constant current driving circuit of infrared diode provides a stable light source for optical rainfall sensor. The stability of the light source will directly affect the detection accuracy of the system. In order to maintain the stability, the circuit has joined the constant current measures. The high speed linear array CCD receives the light signal from the front-end. The size of the object can be judged by the occlusion of the pixels in the linear array. The output signal of the high speed linear array CCD is the full differential LVDS signal. The system adds an external LVDS decoder chip which completes LVDS decoding to save the internal resources of FPGA. After the FPGA receives the original data, the data is processed with corresponding algorithm binarization, which can reduce the data pressure. The data is sent to the ARM9 processor through the external bus after the processing of FPGA, and the ARM9 processor is responsible for data forwarding and system monitoring.

3.1 High speed linear array CCD acquisition module

It is significant of the selection of high speed linear array camera will be directly related to the optical rainfall sensor index and the back-end processingsystem[3]. The basic principle of the high speed linear CCD camera: the camera's part of pixels will be occluded when the rain drops, as shown in Fig 4.

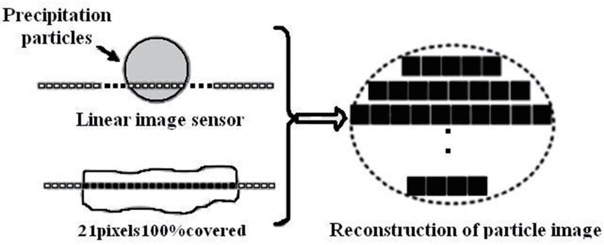

Fig. 4 Raindrop occlusion of linear array CCD camera

The diameter of raindrops can be obtained for using the occluded CCD element[4]. The minimum rain detection is 0.1mm in this design. According to the sampling theorem, the sampling frequency of the signal must be at least 2 times of the highest frequency component of the original signal to ensure that the sampled signal truly retain the original analog signal. The unit pixel size is at least smaller than 50μm. And considering band instabilities and discreteness, the unit pixel size is smaller than 25μm. For the maximum speed of rain drop is 20m/s, the time for it to pass through light band is so short and the scanning speed of the camera can't meet the requirements. It is suitable for choosing the high speed linear array CCD camera[5]. In addition, the size of a single pixel camera determines the resolution of raindrops. After the comparison of the data, the P4-CM-02K10D-00-R CCD camera of Teledyne Dalsa is selected. The CCD camera resolution is 2048×2. The unit pixel size is 10.56 μm ×10.56 μm. The TDI mode can reach 100 KHz for line scan rate. And it supports Camera Link protocol. All the technical indexes meet the design requirements.

P4-CM-02K10D-00-R CCD camera has two Camera Link interface with 26 pins each and all the output and received signal is LVDS. The camera's configuration signal is connected with FPGA chip from CC1 to CC4. The three signals (X0 to X3, Y0 to Y3, Z0 to Z3) are the output of the LVDS signal. The pins link the three DS90C288, and the high-speed LVDS data is converted into a low speed TTL level signal by DS90C288. XCLK, YCLK and ZCLK are the clock's output clock and link the differential clock pin of DS90C288. The three clock pins control the read timing of DS90C288.

3.2 LVDS decoding module

The output of CCD camera is LVDS whose signal rate is up to 100 KHz. And the data can be 8-bit, 10-bit or 12-bit, but this design selects 8-bit output[6]. A row of pixels is 2048 and the data volume of the back-end FPGA can be estimated.

$$m = f \times w \times l = 1.6 \text{ Gbits/s}$$

In the formula, m is the data volume of the back-end and f stands for line frequency. W is the width of one pixel and l is the number of pixels for one row.

Therefore, the large data volume leads to heavy processing burden of back-end FPGA[7]. Considering the PCB layout of the whole system and the burden of FPGA program, the final decision is to add LVDS of DS90C288 between CCD camera and FPGA chip. The high speed differential signal of CCD output can be decoded into a 20-85MHz low speed CMOS/TTL level signal by this chip. That is to say, the four received LVDS signals are demodulated into the 28-bit COMS/TTL level signal. And the connection diagram is shown in Fig 5.

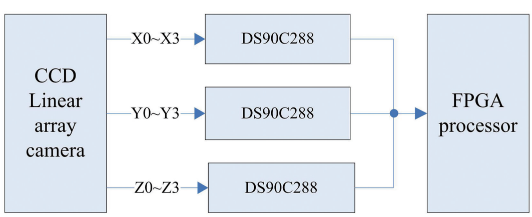

Fig. 5 LVDS decode circuit

The differential receiver pin of DS90C288 is connected with the differential output pin of camera. The COMS/TLL level output pin (the demodulator output pin) of DS90C288 links the FPGA chip. At the same time, the LDVS signal transmission hardware design needs the terminal match for LVDS signal to reduce the reflection and ensure integrity. Therefore, a 100 ohm resistor is required among the differential signal lines of LVDS receiving end in this hardware design.

3.3 Data processing module

The sampling rate of the CCD camera is so fast that the amount of data reaches 1.6 Gbis/s. And effective rainfall information is few, so the collected rainfall signal needs data compression processing in the FPGA part to extract the useful rainfall signal. This will have a very high requirement for the data processing ability, speed and storage space. In order to have more space for data processing, the design uses high-end Altera stratix III EP3SE50F484N. The chip has 19K adaptive logical module (ALMs), 47.5K logical unit (LEs), 400 M9K blocks, 12 M144K blocks, 4 analog phase locked loops (PPL), 48 DSP modules and 5625K bits RAM48. No matter the speed or the internal RAM space, this meets the design requirements[8].

3.4 ARM9 kernel control module

ARM9 kernel control module mainly achieves the following processing of rainfall information, the network communication with the PC and the system self-checking. The tasks of this part are heavy, and thesystem needs to be transplanted in the control chip to facilitate the operation and management of the task. Finally, the S3C2440 of ARM9 is selected with two 256MByte SDRAM and one 32MByte NAND FLASH. The diagram is shown in Fig 6.

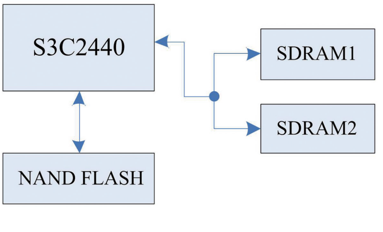

Fig. 6 ARM9 kernel module

S3C2440A is a 32-bit microprocessor of Samsung Corporation that is small and has low power consumption and abundant on-chip peripherals. S3C2440A is based on the ARM920T core supporting MMU, and AMBA bus structure and Harvard high speed buffer structure are adopted, which have 16 KB high speed data and instruction cache. The following functions are supported by S3C2440A. The integrated external memory controller is easy to expand external memory, integrate four-channel DMA and improve the core data processing ability. The Linux, WINCE and other operating system can run in this system. A variety of serial communications are supported, including one-channel IIC, one-channel IIS, two-channel SPI and three send/receive FIFO internal UART with 64 bytes. SD card interface protocol and MMC card protocol are supported as well as three-channel USB interface. The eight-channel and 10-bit ADC and high precision RTC clock are available. And 60 interrupt sources which contain 24 external interrupt sources, having more than 130 functional reuse IO ports. In addition, S3C2440A also supports the little-endian and big-endian storage mode, 4KB starting buffer, NAND flash start-up and eight programmable data bus BANK spaces each for 128 M.

The K9F2G08 of Samsung whose storage capacity is 256 M×8 bit is used as system Flash and it is a popular NAND flash in theembedded field. Compared with Nor Flash, it has the advantages of small size, large memory capacity and more times for erasing. It can be started from NAND flash. At the beginning, the first 4K bytes of NAND flash will be loaded into the inside SRAM buffer of the S3C2440 which is called "starting stone". After the EEC check, the rest code stored in the NAND flash is copied to the SDRAM to complete starting process. Some preconditions are required for automatic NAND flash start-up as follows. Both OM0 and OM1 need to be low level to boot the NAND flash. According to the specific NAND flash model, the NCON pin is selected for advanced/general memory. The GPG13 pin is responsible for memory page capacity. The GPG14 pin is selected for memory address period. The GPG15 is the high or low level to decide the width of memory bus.

The maximum addressing space of S3C2440 is 1GB, divided into 8 pieces of the same size address segment called BANK. Except that BANK0 only selects 16-bit or 32-bit bus width, the other 7 BANKs all support 8-bit/16-bit/32-bit programmable bus width. All BANKs support external ROM and SRAM, and BANK6 and BANK7 also supports external SDRAM. So the system's memory can be extended for external SDRAM on BANK6 and BANK7. This design uses the 32M 48LC16M16A2 as the system RAM. Since there are few SDRAM products in the market, 32-bit SDRAM as the combination of two pieces of 16-bit 48LC16M162A maximizes the performance of S3C2440 processor .

3.5 Ethernet module

The whole system communicates with PC terminal through Ethernet and the DM9000A of DAVICOM isused. The chip can link microprocessor (MPU) and single chip microcomputer (MCU) in many ways (ISA bus), supporting 10/100M rate. It also has a 10/100M adaptive PHY and 4K DWORD value of SRAM. Moreover, it provides a medium-free interface to connect all the home telephone line network equipment or other transceiver. The 8-bit, 16-bit and 32-bit interfaces are supported by the DM9000A to visit internal memory and sustain different processors. The physical protocol layer interface of DM9000A fully supports the use of 3 types, 4 types and 5 types Unshielded Twisted-Pair (UTP) under 10MBps and the use of 5 types UTP, which completely complies with IEEE 802.3u standard. Its automatic coordination function will configure the line bandwidth at the maximum limit. Furthermore, this chip supports full-duplex flow control for IEEE 802.3x. The circuit diagram is shown in Fig 7.

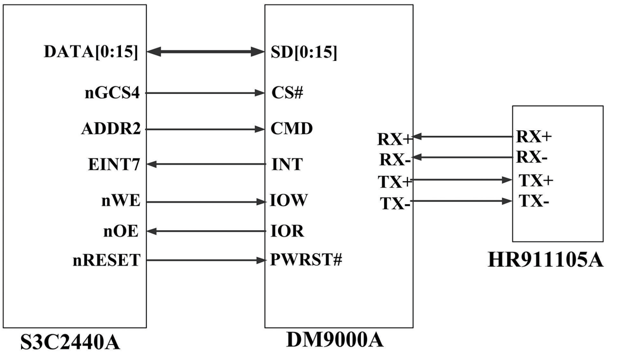

Fig. 7 DM9000 circuit diagram

The PCB of the network interface is a key point of the hardware design of the system. The layout of send and receive differential lines and the separation of the analog and digital ground should be noticed[9]. And it is important to pay attention to the use of power filter capacitor. The references for layout of network interface are shown in Fig 8.

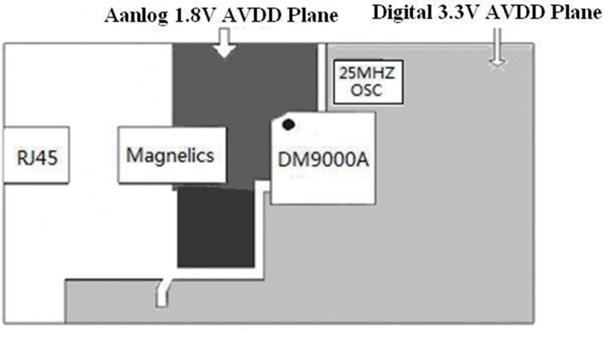

Fig. 8 DM9000C PCB layout

4 Two-dimensional space raindrops algorithm

The method in two-dimensional space is to solve the overlap problem in one-dimensional-space[10]. When two overlapping raindrops appear on the X axis, the X axis only considers existing one rain drop, which comes up with the calculation error. In order to solve the overlapping problem on the same axis, the Y axis is introduced. A number of raindrops can be found in the CCD of Y axis. The diameter of raindrops can be obtained by using the one-dimensional space method on X and Y axis and finally the rainfall can be calculated.

It is assumed that rain is a spherical particle when it falls through linear CCD band[11], as shown in Fig 9. When the rain decreased through band, the high-speed CCD finds n lines and Δt is the reciprocal of linear array CCD horizontal frequency f. The collected images from linear array CCD processed by binarization are stored into RAM. Through the process, the longest line is found. The width of each pixel is known, so diameter of the spherical particle can be calculated, which is suitable for the 2.5 mm rain drops.

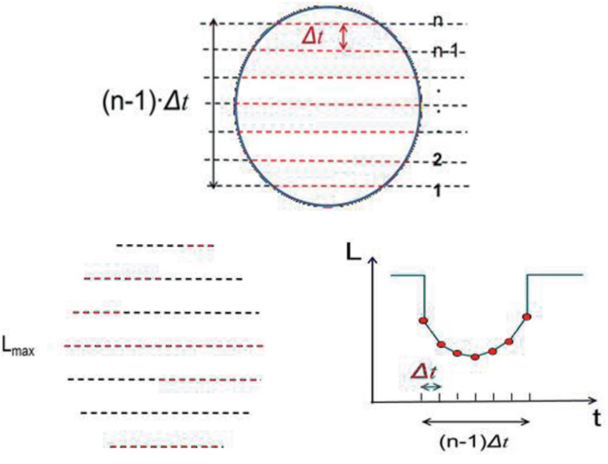

Fig. 9 Spherical particle raindrop diagram

Assuming the width ofone single[12] pixel is W and the number of raindrops in the L_{MAX} is C.

The diameter of a rain drop d: $d = C \times W$

The amount of rainfallfrom one single[13] drop:

$$p = \frac{4}{3}\pi R^3 = \frac{1}{6}\pi d^3$$

The approximate calculation ofrainfall[14] rate V:

$$\Delta t = \frac{1}{f} n = \frac{d \times f}{V}$$

So the rainfall rate: $V = \frac{d \times f}{n} = \frac{d}{n \times \Delta t}$

When the diameter of raindrops issmaller than 2.5mm, the shape of raindrops is more[15] like an ellipsoid. At this point, the amount of rainfall should be calculated in the way of an ellipsoid. The image of Raindrops falling through band is shown in Figure 10.

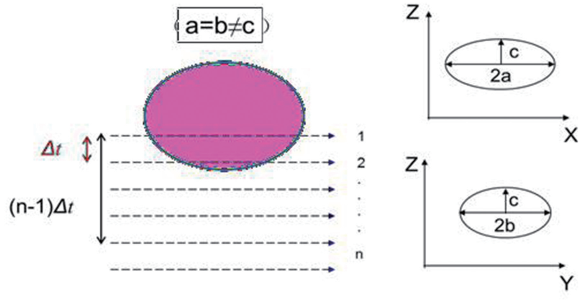

Fig. 10 Ellipsoid raindrop

The amount of rainfall converted into ellipsoid:

$$p = \frac{4}{3}\pi a \times b \times c$$

5 System test

The rainfall Simulates with drop experiment. After the CCD acquisition and FPGA image decoding processing, the reproduced image of rain drops on the VGA display device. Through the image from the end of the ARM9 image processing algorithm, the one-dimensional drop´s diameter is obtained. The collected images are shown in Fig 11.

Fig. 11 Image data after processing

6 Conclusion

It solves the problem of environmental adaptability of the rain gauge by using the method of high speed linear array CCD to measure the velocity and diameter of raindrops. The method of two-dimensional space method can solve the overlapping error of the rain drops in the one-dimensional space, achieve a more accurate calculation. However, there are some problems in the two-dimensional model. The structure is complex and the multiple light sources are inconsistent. These measurement errors have been found. Meanwhile, it is difficult to detect small raindrops due to the uneven light path. The problems need to be improved in the further research.

Acknowledgment

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Authors' Biographies

YANG Bifeng, born in 1980, now is an associate professor in Chengdu University of Information Technology. His research interests include atmospheric sounding technology and application, signal acquisition technology and application.

Tel: +86-028-85966010

E-mail: ybfjs@cuit.edu.cn